

**PETITION FOR REISSUED PATENT AND DECLARATION
COMBINED WITH AUTHORIZATION OF AGENT**

 X REGULAR (UTILITY) OR _____ DESIGN APPLICATION
(check one)

Attorney Docket
No.: SC10098C

As one of the undersigned joint inventors, I hereby declare that:

1. My residence, post office address and citizenship are as stated below with my signature.

2. I believe that we are the original, first and joint inventors of the subject matter which is claimed in U.S. Patent No. 5,859,768, issued January 12, 1999, and which is additionally claimed in the preliminary amendment which is attached to this application, and for which a reissued patent is hereby sought on the invention entitled: POWER CONVERSION INTEGRATED CIRCUIT AND METHOD FOR PROGRAMMING, the specification of which:

(check one) X is attached hereto.
_____ was filed on _____ as
U.S. Application Serial No. _____
and was amended on _____
(if applicable)

3. I hereby state that I have reviewed and understand the contents of the above identified application, including the claims and that I have reviewed and understand the contents of the attached preliminary amendment, including the claims.

4. I acknowledge my duty to disclose information of which I am or became aware which may be material to the patentability of this application. I understand that no patent will be granted on an application in connection with which fraud on the Office has been attempted or the duty of disclosure violated through bad faith or gross negligence. 37 C.F.R. §1.56.

5. I hereby declare that I do not know that, and do not believe that, the claimed subject matter of this application was:

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ever known or used in the United States before our invention thereof,

patented or described in any printed publication in any country before our invention thereof or more than one year prior to the date of the original application,

in public use or on sale in the United States more than one year prior to the date of the original application, or

patented or made the subject of an inventor's certificate in any country foreign to the United States or an application filed by me or my legal representatives or assigns more than twelve months prior to the date of the original application.

6. I further declare that U.S. Patent No. 5,859,768 as issued on January 12, 1999 is partially inoperative because it includes claims that are insufficient to claim all that we had a right to claim. In particular:

a. Claims 1-20 do not adequately claim an external state mode control mechanism or its effect during power conversion. The claims as allowed, for instance, would not constitute literal infringement of a device accepting external state control signals which controls power conversion over multiple cycles of a switching signal in order to implement a power conservation mode.

7. Although claims 1-20 reflect various correct detailed embodiments of our invention, these claims are insufficient to fully claim what was invented by us and disclosed in the specification of our issued U.S. Patent. In particular, the issued U.S. Patent fails to include a claim directed to providing an external state control signal to the power conversion circuit which alters the switching signal of the power conversion circuit over multiple cycles of the switching signal to reduce power conversion of the power converter.

8. Despite the absence of claims to this effect in the issued U.S. Patent, the specification fully supports these claims.

a. The specification of the issued patent speaks of an embodiment beginning at column 6, line 54, and continuing to column 7, line 43. The embodiment describes a connection of a microprocessor, for example, to the power conversion integrated circuit 44 state pin 48. FIG. 4 displays a microprocessor interface switch circuit 100 for use with a state circuit 50 shown in FIG. 2 for controlling the operation of power supply 10 in FIG. 1. Thus, the specification sets forth an embodiment which allows external state control of the operation of a power supply using a microprocessor interface switch circuit.

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PTO/SB/53 (10-00)

Approved for use through 12/30/2000. OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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REISSUE APPLICATION: CONSENT OF ASSIGNEE; STATEMENT OF NON-ASSIGNMENT		Docket Number (Optional) SC10098C
This is part of the application for a reissue patent based on the original patent identified below.		
Name of Patentee(s) Jefferson W. Hall, Jade H. Alberkrack		
Patent Number 5,859,768	Date Patent Issued January 12, 1999	
Title of Invention Power Conversion Integrated Circuit And Method For Programming		
<p>1. <input checked="" type="checkbox"/> Filed herein is a statement under 37 CFR 3.73(b). (Form PTO/SB/96)</p> <p>2. <input type="checkbox"/> Ownership of the patent is in the inventor(s), and no assignment of the patent is in effect.</p> <p>One of boxes 1 or 2 above must be checked. If multiple assignees, complete this form for each assignee. If box 2 is checked, skip the next entry and go directly to "Name of Assignee".</p> <p>The written consent of all assignees and inventors owning an undivided interest in the original patent is included in this application for reissue.</p>		
The assignee(s) owning an undivided interest in said original patent is/are <u>Semiconductor Components Industries, LLC</u> , and the assignee(s) consents to the accompanying application for reissue.		
Name of assignee/inventor (if not assigned) Semiconductor Components Industries, LLC		
Signature <i>William L. George</i>	Date Oct 30, 2000	
Typed or printed name and title of person signing for assignee (if assigned) William L. George Sr. V.P. & Chief Mfg & Tech Officer		

Burden Hour Statement: This form is estimated to take 0.1 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

09/709893



11/13/00

For good and valuable consideration, the receipt of which hereby acknowledged, we, Jefferson W. Hall of Phoenix, AZ and Jade H. Alberkrack of Tempe, AZ, have sold, assigned and transferred, and do hereby sell, assign and transfer unto MOTOROLA, INC., a corporation of the State of Delaware, having its principal office in Schaumburg, State of Illinois, United States of America, and its successors, assigns, and legal representatives, the entire right, title and interest for the United States of America in and to certain inventions relating to improvements in **POWER CONVERSION INTEGRATED CIRCUIT AND METHOD FOR PROGRAMMING** (Attorney Docket No. SC10098C), described, illustrated and claimed in an application for Letters Patent of the United States of America executed by us, together with the entire right, title and interest in and to the application, and in and to Letters Patent which may be issued upon the application, and upon any division, extension, continuation, or reissue thereof.

We hereby also sell, assign and transfer unto MOTOROLA, INC., the entire right, title and interest in and to the invention and in and to applications for Letters Patent therefor in all countries foreign to the United States of America, including all rights under any and all international conventions and treaties in respect of the inventions and the applications for Letters Patent in foreign countries, and we further authorize MOTOROLA, INC. to apply for Letters Patent in foreign countries directly in its own name, and to claim the priority of the filing date of the application for Letters Patent of the United States of America under the provisions of any and all international conventions and treaties.

We hereby authorize and request the Commissioner of Patents and Trademarks of the United States of America to issue Letters Patent upon the aforesaid application, division, extension, continuation or reissue, to MOTOROLA, INC., for the sole use and behoof of MOTOROLA, INC., its successors, assigns and legal representatives, to the full end of the term for which the Letters Patent may be granted, the same as they would have been held and enjoyed by us had this assignment not been made, and we hereby authorize and request the equivalent authorities in foreign countries to issue the patents of their respective countries to MOTOROLA, INC.

We agree that, when requested, we will, without charge to MOTOROLA, INC., but at its expense, sign all papers, take all rightful oaths, and do all acts which may be necessary, desirable or convenient for securing and maintaining patents for the inventions in any and all countries and for vesting title thereto in MOTOROLA, INC., its successors, assigns and legal representatives or nominees.

We covenant with MOTOROLA, INC., its successors, assigns and legal representatives, that the interest and property hereby conveyed is free from all prior assignment, grant, mortgage, license or other encumbrance.

Jefferson W. Hall
Jefferson W. Hall

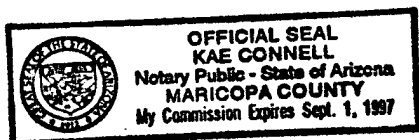
Jade H. Alberkrack
Jade H. Alberkrack

STATE OF ARIZONA)

COUNTY OF MARICOPA)

I, Kae Connell, a Notary Public in and for the County and State aforesaid, do hereby certify that Jefferson W. Hall and Jade H. Alberkrack, whose name(s) are subscribed to the foregoing instrument, appeared before me this day in person and acknowledged that he/she signed, sealed and delivered the instrument as his/her free and voluntary act and deed for the uses and purposes therein set forth.

Given under my hand and notarial seal this 30 day of May, 1997.



Kae Connell
My commission expires on _____

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Address correspondence concerning this document to: Motorola, Inc., Intellectual Property Department - Suite R3108, P.O. Box 10219, Scottsdale, Arizona 85271-0219.

Recorded 4/24/00
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Mailed 4-19-00 USPTO
PTO REC'd 4-24-00

ASSIGNMENT

(16 pages)

In consideration of good and valuable consideration, receipt of which is hereby acknowledged, Motorola, Inc., a corporation of the state of Delaware, having its principal offices in Schaumburg, State of Illinois, United States of America, (the "Assignor") have sold, assigned, and transferred, and does hereby sell, assign, and transfer to Semiconductor Components Industries, L.L.C., a corporation of the state of Delaware, having its principal offices in Phoenix, State of Arizona, United States of America (the "Assignee"), and its successors, assigns, and legal representatives, its entire right, title, and interest for the United States of America, in and to certain inventions described, illustrated, and claimed in any and all patent applications as listed in attached Schedule A (hereinafter "Inventions"), in any and all Letters Patents issuing therefor, and in any and all continuing applications, divisionals, continuations-in-part, reissues, extensions, renewals, reexaminations, and substitutes of such applications or Letters Patents to the full end of the term or terms for which such Letters Patents issue, such entire right, title, and interest to be held and enjoyed by the above-named Assignee to the same extent as they would have been held and enjoyed by the Assignor had this assignment and sale not been made.

Assignor does hereby also sell, assign, and transfer unto Assignee the entire right, title, and interest in and to the Inventions and in and to applications for Letters Patent therefor, in any and all Letters Patents issuing therefor, and in any and all continuing applications, divisionals, continuations-in-part, reissues, extensions, renewals, reexaminations, and substitutes of such applications or Letters Patents to the full end of the term or terms for which such Letters Patents issue, in all countries foreign to the United States of America, including all rights under any and all international conventions and treaties in respect of the Inventions and the applications for Letters Patent in foreign countries. Assignor further authorizes Assignee to apply for Letters Patent in foreign countries directly in its own name, and to claim the priority of the filing date of the application for Letters Patent of the United States of America under the provisions of any and all international conventions and treaties.

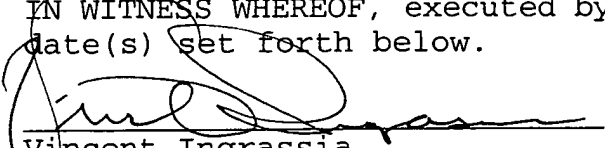
Assignor agrees to execute all papers and assist Assignee as necessary, at Assignee's expense, in connection with the assignment of the applications and any continuing applications, divisionals, continuations-in-part, reissues, extensions, renewals, reexaminations, and substitutes of such applications. Assignor agrees to execute all papers and cooperate with Assignee as necessary, at Assignee's expense, in connection with any interference that may be declared concerning the applications or any continuing applications, divisionals, continuations-in-part,

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reissues, extensions, renewals, reexaminations, and substitutes of such applications.

Assignor hereby represents that Assignor has full right and authority to convey the entire right, title, and interest herein assigned, and that Assignor has not executed, and will not execute, any agreement in conflict therewith.

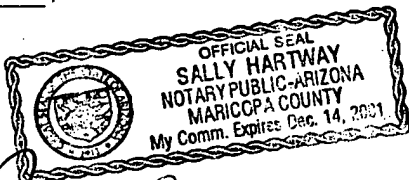
IN WITNESS WHEREOF, executed by the Assignor and Assignee on the date(s) set forth below.


Vincent Ingrassia
Motorola, Inc.


STATE OF ARIZONA)
COUNTY OF MARICOPA)

I, Sally Hartway, a Notary Public in and for the County and State aforesaid, do hereby certify that Vincent Ingrassia, whose name(s) are subscribed to the foregoing instrument, appeared before me this day in person and acknowledged that he/she signed, sealed and delivered the instrument as his/her free and voluntary act and deed for the uses and purposes therein set forth.

Given under my hand and notarial seal this 14th day of April, 2000.




My commission expires on 12-14-01


Bill George

Semiconductor Components Industries, L.L.C.

STATE OF ARIZONA)
COUNTY OF MARICOPA)

I, Tracy Hewelt, a Notary Public in and for the County and State aforesaid, do hereby certify that Bill George, whose name(s) are subscribed to the foregoing instrument, appeared before me this day in person and acknowledged that he/she signed, sealed and delivered the instrument as his/her free and voluntary act and deed for the uses and purposes therein set forth.

Given under my hand and notarial seal this 21st day of March, 2000.




My commission expires on 3-2-02

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UNITED STATES PATENTS AND PATENT APPLICATIONS

Reassignment from Motorola, Inc. to Semiconductor Components Industries L.L.C.

FILE DATE	APPLN. #	GRANT Dt.	PATENT N.	TITLE
7/14/1989	380064 ✓	8/6/1991	5038054	PROTECTED DARLINGTON TRANSISTOR ARRANGEMENT
10/4/1989	417137 ✓	6/25/1991	5027010	TTL OUTPUT DRIVER HAVING AN INCREASED HIGH OUTPUT LEVEL
7/2/1990	546636 ✓	7/2/1991	5029295	BANDGAP VOLTAGE REFERENCE USING A POWER SUPPLY INDEPENDENT CURRENT SOURCE
5/29/1990	529833 ✓	8/6/1991	5038057	AN ECL TO CMOS LOGIC TRANSLATOR
5/11/1992	884319 ✓	7/18/1995	5434442	FIELD PLATE AVALANCHE DIODE
6/4/1990	533231 ✓	11/5/1991	5063311	PROGRAMMABLE DELAY CIRCUIT FOR DIGITAL INTEGRATED CIRCUITS
11/6/1990	609560 ✓	8/6/1991	5038058	BICMOS TTL OUTPUT DRIVER
12/6/1993	08/161559 ✓	8/22/1995	5444395	NON-SATURATING BIPOLAR TRANSISTOR CIRCUIT
12/12/1994	08/354384 ✓			SEMICONDUCTOR DEVICE WITH FLAME SPRAYED HEAT SPREADING LAYER AND METHOD
11/3/1997	08/962725 ✓			POWER MOSFET DEVICE HAVING LOW ON-RESISTANCE AND METHOD
3/4/1998	09/033628 ✓			SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
12/21/1998	09/217120 ✓			SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE
4/7/1999	09/287279 ✓			SYNCHRONOUS RECTIFIER AND METHOD OF OPERATION
5/9/1980	148096 ✓	8/24/1982	4346310	VOLTAGE BOOSTER CIRCUIT 5.2E MOS CMOS
3/27/1990	499845 ✓	5/26/1992	RE33941	POWER DRIVER HAVING SHORT CIRCUIT PROTECTION
8/15/1988	232190 ✓	3/28/1989	4816739	DC/DC CONVERTER
12/24/1990	630804 ✓	10/22/1991	5060047	HIGH VOLTAGE SEMICONDUCTOR DEVICE
10/6/1995	08/539900 ✓	4/1/1997	5616971	POWER SWITCHING CIRCUIT
7/16/1982	399028 ✓	6/5/1984	4453095	ECL MOS BUFFER CIRCUITS
8/24/1981	295880 ✓	9/6/1983	4403200	OUTPUT STAGE FOR OPERATIONAL AMPLIFIER
8/17/1981	293753 ✓	11/22/1983	4417216	OPERATIONAL AMPLIFIER
10/26/1981	315085 ✓	7/12/1983	4393355	OPERATIONAL AMPLIFIER
5/27/1982	382754 ✓	11/24/1987	4709171	CURRENT LIMITER & METHOD FOR LIMITING CURRENT
12/9/1982	447928 ✓	12/4/1984	4486880	OUTPUT MULTIPLEXER HAVING ONE GATE DELAY
5/13/1983	494201 ✓	6/12/1984	4454454	MOSFET "H" SWITCH CIRCUIT FOR A DC MOTOR
8/22/1983	525196 ✓	11/12/1985	4553041	MONOLITHIC ZERO CROSSING TRIAC DRIVER
3/12/1997	08/820428 ✓			SURFACE MOUNT SEMICONDUCTOR DIODE DEVICE
2/4/1986	825954 ✓	10/6/1987	4698655	OVERVOLTAGE AND OVERTEMPERATURE PROTECTION CIRCUIT

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Schedule A

UNITED STATES PATENTS AND PATENT APPLICATIONS

~~Reassignment from Motorola, Inc. to Semiconductor Components Industries L.L.C.~~

				METHOD FOR PRODUCING LOW NOISE, HIGH GRADE CONSTANT SEMICONDUCTOR JUNCTIONS
3/12/1984	588628	3/22/1988	4732866	
4/2/1984	595764	11/12/1985	4553084	CURRENT SENSING CIRCUIT
4/28/1986	856258	7/28/1987	4683442	METHOD FOR RESISTOR TRIMMING BY METAL MIGRATION
4/28/1986	856257	9/26/1989	4870472	METHOD FOR RESISTOR TRIMMING BY METAL MIGRATION
3/19/1984	590948	8/27/1985	4538116	IMPROVED OUTPUT STAGE FOR AN OPERATIONAL AMPLIFIER
9/10/1984	649081	3/3/1987	D288557	SEMICONDUCTOR HOUSING
3/26/1984	593165	11/12/1985	4553106	IMPROVED OUTPUT STAGE FOR AN OPERATIONAL AMPLIFIER
				CURRENT LIMIT TECHNIQUE FOR MULTIPLE-EMITTER VERTICAL POWER TRANSISTOR
2/22/1984	582360	8/6/1985	4533845	
11/28/1986	936919	7/12/1988	4757025	METHOD OF MAKING GATE TURN OFF SWITCH WITH ANODE SHORT AND BURIED BASE
				TRIMMABLE DIFFERENTIAL AMPLIFIER HAVING A ZERO TEMPERATURE COEFFICIENT OFFSET
6/30/1986	880391	2/9/1988	4724397	
1/16/1986	819320	1/5/1988	4717641	METHOD FOR PASSIVATING A SEMICONDUCTOR JUNCTION
6/24/1985	748362	2/17/1987	4644194	ECL TO TTL VOLTAGE LEVEL TRANSLATOR
1/3/1986	815963	3/3/1987	4648021	FREQUENCY DOUBLER CIRCUIT AND METHOD
				MONOLITHIC TEMPERATURE COMPENSATED VOLTAGE-REFERENCE DIODE AND METHOD FOR ITS
8/6/1985	762751	9/26/1989	4870467	
				MONOLITHIC TEMPERATURE COMPENSATED VOLTAGE-REFERENCE DIODE AND METHOD FOR ITS
7/3/1989	375236	12/12/1989	4886762	
4/7/1986	849090	1/5/1988	4717890	SYMMETRIC LAYOUT FOR QUAD OPERATIONAL AMPLIFIERS
5/5/1986	859690	12/29/1987	4716510	AUTOMATIC RESTART CIRCUIT FOR A SWITCHING POWER SUPPLY
7/27/1987	80258	2/16/1988	4725912	POWER MOS LOSS OF GROUND PROTECTION
				METHOD OF MAKING VERTICAL FIELD EFFECT TRANSISTOR WITH PLURALITY OF GATE INPUT
5/4/1987	45502	7/12/1988	4757029	
6/30/1986	880534	11/24/1987	4709216	OPERATIONAL AMPLIFIER WITH PASSIVE CURRENT LIMITING
6/30/1986	880251	12/1/1987	4710728	AMPLIFIER HAVING IMPROVED GAIN BANDWIDTH PRODUCT
				DIFFERENTIAL AMPLIFIER INCLUDING BALANCED TWO TERMINAL SERIES RC NETWORK
6/30/1986	880472	12/29/1987	4716379	

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UNITED STATES PATENTS AND PATENT APPLICATIONS

Reassignment from Motorola, Inc. to Semiconductor Components Industries L.L.C.

4/3/1987	33959	6/7/1988	4749883	CIRCUIT HAVING AN OUTPUT REFERENCED TO A SPECIFIC VOLTAGE IN RESPONSE TO EITHER AN
9/18/1986	908858	2/16/1988	4725791	CIRCUIT UTILIZING RESISTORS TRIMMED BY METAL MIGRATION
11/17/1986	931309	3/1/1988	4727912	LEAD STRAIGHTENER AND FLATTENER FOR SEMICONDUCTOR DEVICES
6/1/1987	56166	10/4/1988	4775643	MESA ZENER DIODE AND METHOD OF MANUFACTURE THEREOF
12/24/1986	946349	4/5/1988	4736126	TRIMMABLE CURRENT SOURCE
12/29/1986	947127	12/15/1987	4713626	OPERATIONAL AMPLIFIER UTILIZING JFET FOLLOWERS
9/22/1986	909808	1/5/1988	4717885	OPERATIONAL AMPLIFIER UTILIZING FET FOLLOWERS AND FEED-FORWARD CAPACITORS
6/30/1986	880537	1/5/1988	4717886	OPERATIONAL AMPLIFIER UTILIZING RESISTORS TRIMMED BY METAL MIGRATION
12/22/1986	944048	1/26/1988	4721921	AMPLIFIER HAVING IMPROVED GAIN/BANDWIDTH PRODUCT
11/23/1987	124212	11/8/1988	4783428	METHOD OF PRODUCING A THERMOGENETIC SEMICONDUCTOR DEVICE
12/28/1987	138262	6/6/1989	4837177	BIPOLAR SEMICONDUCTOR DEVICE HAVING A CONDUCTIVE RECOMBINATION LAYER
2/21/1989	312268	11/14/1989	4881115	BIPOLAR SEMICONDUCTOR DEVICE HAVING A CONDUCTIVE RECOMBINATION LAYER
3/18/1987	27366	10/4/1988	4775879	FET STRUCTURE ARRANGEMENT HAVING LOW ON RESISTANCE
8/29/1988	237370	12/25/1990	4980579	ECL GATE HAVING DUMMY LOAD FOR SUBSTANTIALLY REDUCING SKEW
1/31/1991	648072	3/31/1992	5100829	SEMICONDUCTOR STRUCTURE WITH CLOSELY COUPLED SUBSTRATE TEMPERATURE SENSE
9/9/1988	243363	3/19/1991	5001545	FORMED TOP CONTACT FOR NON-FLAT SEMICONDUCTOR DEVICE
2/12/1990	478852	5/5/1992	5110761	FORMED TOP CONTACT FOR NON-FLAT SEMICONDUCTOR DEVICES
11/10/1987	118927	4/25/1989	4825144	DUAL CHANNEL CURRENT MODE SWITCHING REGULATOR
12/7/1987	129505	3/21/1989	4814852	CONTROLLED VOLTAGE DROP DIODE
5/23/1988	197784	5/9/1989	4829265	OPERATIONAL AMPLIFIER
5/22/1989	354574	2/11/1992	5087830	START CIRCUIT FOR A BANDGAP REFERENCE CELL
4/17/1991	687192	8/25/1992	5141887	LOW VOLTAGE DEEP JUNCTION DEVICE AND METHOD
7/7/1988	215978	10/3/1989	4871929	ECL LOGIC GATE

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UNITED STATES PATENTS AND PATENT APPLICATIONS

~~Reassignment from Motorola, Inc. to Semiconductor Components Industries L.L.C.~~

3/14/1989	322845	8/7/1990	4946518	METHOD FOR IMPROVING THE ADHESION OF A PLASTIC ENCAPSULANT TO COPPER CONTAINING
4/4/1988	177209	2/28/1989	4808839	POWER FIELD EFFECT TRANSISTOR DRIVER CIRCUIT FOR PROTECTION FROM OVER VOLTAGES
5/16/1988	194356	9/19/1989	4868415	VOLTAGE LEVEL CONVERSION CIRCUIT
3/30/1989	330850	10/2/1990	4960723	SELF ALIGNED VERTICAL FIELD EFFECT TRANSISTOR HAVING AN IMPROVED SOURCE CONTACT
4/23/1999	09/298753			POWER FACTOR CORRECTION CONTROLLER CIRCUIT
9/9/1988	242926	6/19/1990	4935803	SELF-CENTERING ELECTRODE FOR POWER DEVICES
2/9/1990	477397	2/19/1991	4994412	SELF-CENTERING ELECTRODE FOR POWER DEVICES
3/2/1990	489853	11/13/1990	4970173	HIGH VOLTAGE VERTICAL FIELD EFFECT TRANSISTOR WITH IMPROVED SAFE OPERATING AREA
4/6/1989	333938	8/7/1990	4946376	BACKSIDE METALLIZATION SCHEME FOR SEMICONDUCTOR DEVICES
7/19/1989	381871	10/23/1990	4965466	SUBSTRATE INJECTION CLAMP
5/1/1989	345321	5/15/1990	4926073	NEGATIVE VOLTAGE CLAMP
1/31/1994	08/188975	5/20/1997	5631187	METHOD FOR MAKING SEMICONDUCTOR DEVICE HAVING HIGH ENERGY SUSTAINING
2/25/1994	08/202856	11/15/1994	5365099	SEMICONDUCTOR DEVICE HAVING HIGH ENERGY SUSTAINING CAPABILITY AND A TEMPERATURE
4/7/1989	334430	5/1/1990	4922208	OUTPUT STAGE FOR AN OPERATIONAL AMPLIFIER
11/3/1988	266613	8/14/1990	4948991	LOAD CONTROLLED ECL TRANSIENT DRIVER
12/24/1990	632773	3/31/1992	5100821	SEMICONDUCTOR AC SWITCH
10/27/1998	09/179739			INSULATED GATE BIPOLAR TRANSISTOR
7/3/1989	374722	3/5/1991	4998029	DUAL SUPPLY ECL TO TTL TRANSLATOR
10/2/1989	415846	7/3/1990	4939393	AN ECL TO TTL/CMOS TRANSLATOR USING A SINGLE POWER SUPPLY
8/23/1989	397206	12/11/1990	4977107	METHOD FOR MANUFACTURING SEMICONDUCTOR RECTIFIER
12/26/1989	456913	12/18/1990	4978636	METHOD OF MAKING A SEMICONDUCTOR DIODE
8/20/1990	570200	11/19/1991	5066991	METHOD OF MAKING A SEMICONDUCTOR DIODE
11/30/1989	443790	10/22/1991	5059826	VOLTAGE THRESHOLD GENERATOR FOR USE IN DIODE LOAD EMITTER COUPLED LOGIC CIRCUITS
12/18/1989	452080	9/18/1990	4958122	CURRENT SOURCE REGULATOR
5/17/1991	704683	7/14/1992	5130262	INTERNAL CURRENT LIMIT AND OVER VOLTAGE PROTECTION METHOD

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UNITED STATES PATENTS AND PATENT APPLICATIONS

~~Reassignment from Motorola, Inc. to Semiconductor Components Industries L.L.C.~~

				ALPHA ENHANCEMENT OF A TRANSIS TOR USING B ASE CURRENT FEEDBA CK TO THE EMITTER
12/15/1989	450954	2/19/1991	4994758	
12/14/1989	450507	8/17/1993	5237183	HIGH REVERSE VOLTAGE IGT
				METHOD AND APPARATUS FOR ADJUS TING PLATING SOLUTION FLOW CHA RACTERISTICS AT
1/2/1990	459892	3/19/1991	5000827	
				HIGH VOLTAGE PLANAR EDGE TERMI NATION USING A PUNCH-THROUGH R ETARDING IMPLANT
1/2/1990	459506	7/16/1991	5032878	
				HIGH VOLTAGE PLANAR EDGE TERMI NATION USING A PUNCH-THROUGH R ETARDING IMPLANT
2/26/1991	660485	12/24/1991	5075739	
1/17/1991	642717	6/2/1992	5119148	FAST DAMPER DIODE AND METHOD
				AVALANCHE STRESS PROTECTED SEM ICONDUCTOR DEVICE HAVING VARIA BLE INPUT
1/7/1991	637719	5/19/1992	5115369	
				ZIG-ZAG V-MOS TRANSISTOR STRUC TURE
7/18/1980	170131	3/20/1984	4438448	
				UNIVERSAL POWER SUPPLY MONITOR CIRCUIT
2/5/1990	474908	12/25/1990	4980791	
				INTEGRATED HIGH VOLTAGE TRANSI STORS HAVING MINIMUM TRANSISTO R TO TRANSISTOR
3/16/1990	494652	12/31/1991	5077594	
2/20/1990	481268	2/5/1991	4990863	AMPLIFIER OUTPUT STAGE
				HIGH VOLTAGE BRIDGE INTERFACE FOR AC AND BRUSHLESS DC MOTOR CONTROL
2/26/1990	484946	10/30/1990	4967336	
				DIFFERENTIAL ECL BUS TRI-STATE DETECTION RECEIVER
5/21/1990	526267	12/25/1990	4980581	
				HIGH SPEED ECL TO TTL TRANSLAT OR HAVING A NON-SCHOTTKY CLAMP FOR THE OUTPUT
7/2/1990	547257	3/19/1991	5001370	
				ECL CIRCUIT WITH LOW VOLTAGE/F AST PULL-DOWN
7/31/1990	560916	10/22/1991	5059827	
				AMPLIFIER HAVING TWO OPERATING MODES
7/27/1990	558927	10/22/1991	5059921	
				METHOD FOR PRODUCING SEMICONDU CTOR DEVICES HAVING BULK DEFEC TS THERIN
9/4/1990	577183	11/19/1991	5066359	
				SLOPE COMPENSATION CIRCUIT FOR STABILIZING CURRENT MODE CONV ERTERS
9/4/1990	577350	1/7/1992	5079453	
				LOW VOLTAGE CIRCUIT TO CONTROL HIGH VOLTAGE TRANSISTOR
11/6/1990	609540	4/7/1992	5103148	
10/1/1990	590997	3/1/1994	5291075	FAULT DETECTION CIRCUIT
				A CURRENT THRESHOLD DETECTOR C IRCUIT
11/1/1990	607961	10/15/1991	5057709	
				METHOD OF MAKING ENHANCED INSU LATED GATE BIPOLAR TRANSISTOR
6/17/1991	715864	8/25/1992	5141889	SEMICONDUCTOR DEVICE AND METHO D
12/3/1990	620698	2/18/1992	5089427	

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2/27/1991	661152	9/15/1992	5148061	ECL TO CMOS TRANSLATION AND LATCH LOGIC CIRCUIT
3/4/1991	664896	6/9/1992	5120998	SOURCE TERMINATED TRANSMISSION LINE DRIVER
2/25/1991	660185	6/2/1992	5119000	LOW NOISE MOTOR DRIVE CIRCUIT
5/28/1991	706498	6/29/1993	5223732	INSULATED GATE SEMICONDUCTOR DEVICE WITH REDUCED BASE-TO-SOURCE ELECTRODE
5/6/1991	696405	2/2/1993	5183769	VERTICAL CURRENT FLOW SEMICONDUCTOR DEVICE UTILIZING WAFER BONDING
10/26/1992	966822	6/21/1994	5323059	VERTICAL CURRENT FLOW SEMICONDUCTOR DEVICE UTILIZING WAFER BONDING
8/5/1991	740267	1/12/1993	5178370	CONDUCTIVITY MODULATED INSULATED GATE SEMICONDUCTOR DEVICE
6/3/1991	709471	12/17/1991	5073850	START CIRCUIT FOR A POWER SUPPLY CONTROL INTEGRATED CIRCUIT
6/14/1991	715286	10/13/1992	5155052	VERTICAL FIELD EFFECT TRANSISTOR WITH IMPROVED CONTROL OF LOW RESISTIVITY REGION
8/30/1991	753129	8/18/1992	5140280	RAIL-TO-RAIL OUTPUT STAGE OF AN OPERATIONAL AMPLIFIER
8/30/1991	753128	10/6/1992	5153529	RAIL-TO-RAIL INPUT STAGE OF AN OPERATIONAL AMPLIFIER
11/29/1991	800320	4/20/1993	5204562	TURN OFF DELAY REDUCTION CIRCUIT AND METHOD
8/12/1991	743955	5/5/1992	5111381	H-BRIDGE FLYBACK RECIRCULATOR
12/3/1991	801249	12/10/1996	5583348	METHOD FOR MAKING A SCHOTTKY DIODE THAT IS COMPATIBLE WITH HIGH PERFORMANCE
8/23/1991	749020	10/26/1993	5257155	SHORT-CIRCUIT PROOF FIELD EFFECT TRANSISTOR
3/2/1992	844077	11/30/1993	5266515	FABRICATING DUAL GATE THIN FILM TRANSISTORS
11/12/1991	790795	11/30/1993	5266831	EDGE TERMINATION STRUCTURE
12/13/1991	806197	2/8/1994	5285346	CURRENT DRIVER CONTROL CIRCUIT FOR A POWER DEVICE
11/4/1991	787166	2/22/1994	5289028	HIGH POWER SEMICONDUCTOR DEVICE WITH INTEGRAL ON-STATE VOLTAGE DETECTION
12/23/1991	07/812146	1/17/1995	5382841	SWITCHABLE ACTIVE BUS TERMINATION CIRCUIT
2/21/1992	839413	10/8/1996	5563437	SEMICONDUCTOR DEVICE HAVING A LARGE SENSE VOLTAGE
2/13/1992	834746	9/22/1992	5150176	PN JUNCTION SURGE SUPPRESSOR STRUCTURE WITH MOAT
4/6/1992	864102	7/5/1994	5327016	LOAD CONTROL CIRCUIT INCLUDING AUTOMATIC AC/DC DISCERNMENT
4/27/1992	873855	4/20/1993	5204639	MILLER LOOP COMPENSATION NETWORK WITH CAPACITANCE DRIVE

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7/27/1992	919324	12/14/1993	5270585	OUTPUT DRIVER STAGE WITH TWO T IER CURRENT LIMIT PROTECTION
6/22/1992	902251	1/25/1994	5281832	BIDIRECTIONAL TWO-TERMINAL THY RISTOR
7/31/1992	922718	3/15/1994	5294824	HIGH VOLTAGE TRANSISTOR HAVING REDUCED ON-RESISTANCE
6/8/1992	895067	10/25/1994	5359281	QUICK-START AND OVERVOLTAGE PR OTECTION FOR A SWITCHING REGUL ATOR CIRCUIT
6/28/1993	08/082643	9/6/1994	5345101	HIGH VOLTAGE SEMICONDUCTOR STR UCTURE AND METHOD
12/24/1992	996747	2/15/1994	5286660	METHOD FOR DOPING A SEMICONDC TOR WAFER HAVING A DIFFUSION E NHANCEMENT REGION
3/1/1993	08/024142	7/5/1994	5327100	NEGATIVE SLEW RATE ENHANCEMENT CIRCUIT FOR AN OPERATIONAL AM PLIFIER
10/26/1992	966486	5/10/1994	5311147	HIGH IMPEDANCE OUTPUT DRIVER S TAGE AND METHOD THEREFOR
11/30/1992	983357	2/8/1994	5285170	OPERATIONAL AMPLIFIER WITH ALL NPN TRANSISTOR OUTPUT STAGE
2/2/1993	08/012195	12/13/1994	5373201	POWER TRANSISTOR
4/27/1993	52962	1/3/1995	5378928	PLASTIC ENCAPSULATED MICROELEC TRONIC DEVICE AND METHOD
7/21/1994	08/278205	6/4/1996	5523629	PLASTIC ENCAPSULATED MICROELEC TRONIC DEVICE
6/2/1995	08/459142	7/16/1996	5535510	PLASTIC ENCAPSULATED MICROELEC TRONIC DEVICE AND METHOD
5/3/1993	55581	3/14/1995	5397716	METHOD OF FORMING AN INSULATED GATE SEMICONDUCTOR DEVICE AND DEVICE FORMED
12/2/1994	08/348413	4/2/1996	5504351	AN INSULATED GATE SEMICONDUCTO R DEVICE
2/13/1995	08/387690	9/3/1996	5552742	CIRCUIT FOR CONTROLLING CURREN T FLOW BETWEEN TWO NODES
8/29/1994	08/297075	10/24/1995	5460986	PROCESS FOR MAKNG A POWER MOSF ET DEVICE AND STRUCTURE
6/21/1993	08/078096	12/6/1994	5371415	TWO STAGE GATE DRIVE CIRCUIT F OR A FET
12/3/1993	08/160762	11/1/1994	5361001	CIRCUIT AND METHOD OF PREVIEWI NG ANALOG TRIMMING
12/21/1995	08/576270	1/27/1998	5712581	FULL DIFFERENTIAL DATA QUALIFI CATION CIRCUIT FOR SENSING A L OGIC STATE
7/8/1994	08/272899	3/7/1995	5396097	TRANSISTOR WITH COMMON BASE RE GION
3/3/1994	08/205238	9/19/1995	5451806	METHOD AND DEVICE FOR SENSING SURFACE TEMPERATURE OF AN INSU LATED GATE
8/30/1993	08/113007	11/1/1994	5361048	PULSE WIDTH MODULATOR HAVING A DUTY CYCLE PROPORTIONAL TO THE AMPLITUDE OF AN

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10/25/1993	08/140944	12/19/1995	5477175	OFF-LINE BOOTSTRAP STARTUP CIRCUIT
9/24/1993	08/125729	2/21/1995	5391945	CIRCUIT AND METHOD FOR PROVIDING PHASE SYNCHRONIZATION OF ECL AND TTL/CMOS
12/3/1993	08/160764	12/27/1994	5376875	BATTERY CHARGER STATUS MONITOR CIRCUIT AND METHOD THEREFOR
6/23/1995	08/493945	12/3/1996	5581118	ELECTRONIC SURFACE MOUNT DEVICE AND METHOD FOR MAKING
12/16/1996	08/767438	7/7/1998	5777373	SEMICONDUCTOR STRUCTURE WITH FIELD-LIMITING RINGS AND METHOD FOR MAKING
1/4/1994	08/177689	2/14/1995	5390101	FLYBACK POWER SUPPLY HAVING A VCO CONTROLLED SWITCHING RATE
7/15/1994	08/275551	11/14/1995	5467047	POWER TRANSISTOR RAPID TURN OFF CIRCUIT FOR SAVING POWER
2/24/1995	08/393772	12/30/1997	5703389	VERTICAL IGFET CONFIGURATION HAVING LOW ON-RESISTANCE AND METHOD
7/5/1994	08/270281	1/23/1996	5486718	HIGH VOLTAGE PLANAR EDGE TERMINATION STRUCTURE AND METHOD OF MAKING SAME
9/18/1995	08/529384	2/3/1998	5714396	METHOD OF MAKING A HIGH VOLTAGE PLANAR EDGE TERMINATION STRUCTURE
7/18/1994	08/276373	8/20/1996	5548285	CIRCUIT AND METHOD OF INDICATING DATA HOLD-TIME
8/31/1994	08/298715	10/8/1996	5563594	CIRCUIT AND METHOD OF TIMING DATA TRANSFERS
9/6/1994	08/300905	3/19/1996	5500377	METHOD OF MAKING SURGE SUPPRESSOR SWITCHING DEVICE
8/1/1994	08/283929	4/2/1996	5504448	CIRCUIT LIMIT SENSE CIRCUIT AND METHOD FOR CONTROLLING A TRANSISTOR
12/29/1994	08/368408	4/23/1996	5510735	COMPARATOR CIRCUIT
11/25/1994	08/345655	3/12/1996	5498988	LOW POWER FLIP-FLOP CIRCUIT AND METHOD THEREFOR
11/2/1994	08/333466	3/19/1996	5500624	INPUT STAGE FOR CMOS OPERATIONAL AMPLIFIER AND METHOD THEREOF
9/6/1994	08/300545	3/26/1996	5502370	POWER FACTOR CONTROL CIRCUIT HAVING A BOOST CURRENT FOR INCREASING A SPEED OF A
6/20/1994	08/262305	3/11/1997	5610495	CIRCUIT AND METHOD OF MONITORING BATTERY CELLS
12/18/1995	08/573979	11/26/1996	5578841	VERTICAL MOSFET DEVICE HAVING FRONTSIDE AND BACKSIDE CONTACTS
3/11/1997	08/814684	10/6/1998	5818201	CIRCUIT AND METHOD FOR BATTERY CHARGE CONTROL
7/5/1995	08/498158	12/31/1996	5589408	METHOD OF FORMING AN ALLOYED DRAIN FIELD EFFECT TRANSISTOR AND DEVICE FORMED

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12/5/1994	08/349578	11/28/1995	5471174	AMPLIFIER HAVING AN OUTPUT STAGE WITH BIAS CURRENT CANCELLATION
3/3/1995	08/398265	8/5/1997	5654562	LATCH RESISTANT INSULATED GATE SEMICONDUCTOR DEVICE
3/6/1995	08/398830	6/25/1996	5530284	SEMICONDUCTOR LEADFRAME STRUCTURE COMPATIBLE WITH DIFFERING BOND WIRE MATERIALS
5/30/1995	08/452754	9/24/1996	5557842	METHOD OF MANUFACTURING A SEMICONDUCTOR LEADFRAME STRUCTURE
5/2/1995	08/433883	7/16/1996	5536958	SEMICONDUCTOR DEVICE HAVING HIGH VOLTAGE PROTECTION CAPABILITY
8/3/1995	08/510999	1/28/1997	5598086	PEAK VOLTAGE AND PEAK SLOPE DETECTOR FOR A BATTERY CHARGER CIRCUIT
5/9/1997	08/999889	9/7/1999	5949124	EDGE TERMINATION STRUCTURE
2/5/1996	08/595436	3/31/1998	5734277	OUTPUT CIRCUIT AND METHOD FOR SUPPRESSING SWITCHING NOISE THEREIN
9/29/1995	08/536876	11/4/1997	5684663	PROTECTION ELEMENT AND METHOD FOR PROTECTING A CIRCUIT
8/24/1995	08/518768	9/9/1997	5666046	REFERENCE VOLTAGE CIRCUIT HAVING A SUBSTANTIALLY ZERO TEMPERATURE COEFFICIENT
11/3/1997	08/963322	3/23/1999	5886400	SEMICONDUCTOR DEVICE HAVING AN INSULATING LAYER AND METHOD FOR MAKING
10/3/1995	08/538522	10/7/1997	5675268	OVERCURRENT DETECTION CIRCUIT FOR A POWER MOSFET AND METHOD THEREFOR
11/21/1995	08/560774	5/13/1997	5629536	HIGH VOLTAGE CURRENT LIMITER AND METHOD FOR MAKING
1/2/1997	08/778432	5/12/1998	5751025	HIGH VOLTAGE CURRENT LIMITER AND METHOD FOR MAKING
10/4/1995	08/539207	7/8/1997	5646503	METHOD FOR BALANCING POWER SOURCES AND STRUCTURE THEREFOR
12/18/1995	08/573844	5/12/1998	5751061	SEMICONDUCTOR DIODE DEVICE AND METHOD OF MANUFACTURE
12/4/1995	08/566748	5/6/1997	5627494	HIGH-SIDE CURRENT SENSE AMPLIFIER
2/6/1996	08/596036	11/11/1997	5686857	ZERO CROSSING TRIAC AND METHOD
12/26/1995	08/576983	5/20/1997	5631484	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND TERMINATION STRUCTURE
2/6/1996	08/597307	7/28/1998	5786745	ELECTRONIC PACKAGE AND METHOD
12/18/1995	08/573843	6/1/1999	5908316	METHOD OF PASSIVATING A SEMICONDUCTOR SUBSTRATE
1/22/1996	08/599457	6/30/1998	5773368	METHOD OF ETCHING ADJACENT LAYERS
3/19/1996	08/619446	8/25/1998	5798673	LOW VOLTAGE OPERATIONAL AMPLIFIER BIAS CIRCUIT AND METHOD
3/19/1996	08/618671	3/31/1998	5734296	LOW VOLTAGE OPERATIONAL AMPLIFIER INPUT STAGE AND METHOD

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5/5/1997	08/850307	7/28/1998	5785791	METHOD OF MANUFACTURING SEMICONDUCTOR COMPONENTS
3/4/1996	08/610022	6/2/1998	5760639	VOLTAGE AND CURRENT REFERENCE CIRCUIT WITH A LOW TEMPERATURE COEFFICIENT
4/1/1996	08/617722	5/12/1998	5751052	INDUCTIVE DRIVER CIRCUIT AND METHOD THEREFOR
9/3/1996	08/706886	5/12/1998	5751192	INTEGRATED CIRCUIT AND METHOD FOR GENERATING A TRANSIMPEDANCE FUNCTION
3/19/1996	08/618544	12/16/1997	5699015	LOW VOLTAGE OPERATIONAL AMPLIFIER AND METHOD
5/28/1996	08/654364	7/27/1999	5930652	SEMICONDUCTOR ENCAPSULATION METHOD
7/22/1996	08/684802	5/5/1998	5747371	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE
9/3/1996	08/706879	5/19/1998	5754038	METHOD AND CIRCUIT FOR CURRENT REGULATION
4/6/1998	09/055458			METHOD OF MANUFACTURING SEMICONDUCTOR COMPONENTS
9/24/1996	08/719423	10/6/1998	5818890	METHOD FOR SYNCHRONIZING SIGNALS AND STRUCTURES THEREFOR
8/30/1996	08/706095	3/10/1998	5726597	METHOD AND CIRCUIT FOR REDUCING OFFSET VOLTAGES FOR A DIFFERENTIAL INPUT STAGE
7/7/1997	08/887718			SEMICONDUCTOR DEVICE AND METHOD THEREFOR
3/3/1997	08/811062	7/14/1998	5781129	ADAPTIVE ENCODER CIRCUIT FOR MULTIPLE DATA CHANNELS AND METHOD OF ENCODING
11/25/1996	08/755926			SEMICONDUCTOR DEVICE AND METHOD OF MAKING
1/31/1997	08/791711	8/4/1998	5789951	MONOLITHIC CLAMPING CIRCUIT AND METHOD OF PREVENTING TRANSISTOR AVALANCHE
4/7/1997	08/833437	9/8/1998	5804944	BATTERY PROTECTION SYSTEM AND PROCESS FOR CHARGING A BATTERY
6/24/1998	09/103826	7/6/1999	5920181	BATTERY PROTECTION SYSTEM AND PROCESS FOR CHARGING A BATTERY
3/31/1997	08/829073	9/8/1998	5804869	CLAMP DISPOSED AT EDGE OF A DIELECTRIC STRUCTURE IN A SEMICONDUCTOR DEVICE AND
6/3/1997	08/868337	4/6/1999	5892389	METHOD AND CIRCUIT FOR CURRENT LIMITING OF DC-DC REGULATORS
6/4/1997	08/869297	1/12/1999	5859768	POWER CONVERSION INTEGRATED CIRCUIT AND METHOD FOR PROGRAMMING
3/18/1997	08/819899	5/4/1999	5900772	BANDGAP REFERENCE CIRCUIT AND METHOD
2/2/1998	09/016985	5/18/1999	5904555	METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE

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3/30/1998	09/050164	4/27/1999	5897343	POWER SWITCHING TRENCH MOSFET HAVING ALIGNED SOURCE REGIONS AND METHOD OF
6/1/1998	09/087674			SEMICONDUCTOR COMPONENT AND ME THOD OF MANUFACTURE
12/28/1998	09/221433			SEMICONDUCTOR LEADFRAME ASSEMB LY AND METHOD FOR MANUFACTURING A
7/1/1998	09/108448			ELECTRONIC COMPONENT AND METHO D OF MANUFACTURE
6/29/1998	09/106472			ELECTRONIC COMPONENT AND METHO D OF MANUFACTURE
3/1/1999	09/259602			SEMICONDUCTOR DEVICE AND ME THOD OF MANUFACTURE
12/14/1998	09/210698			POWER CONVERTER CIRCUIT AND ME THOD FOR CONTROLLING
12/21/1998	09/217288			SEMICONDUCTOR LOAD DRIVER CIRC UIT AND METHOD THEREFOR
12/21/1998	09/216763			METHOD OF DRIVING A LOAD AND S EMICONDUCTOR LOAD DRIVER CIRCUI T THEREFOR
2/22/1999	09/253933			LOGIC GATE HAVING TEMPERATURE COMPENSATION AND METHOD
5/12/1999	09/310214			METHOD FOR MANUFACTURING A SEM ICONDUCTOR DEVICE AND SEMICOND UCTOR DEVICE
4/12/1999	09/289807			SWITCHING REGULATOR FOR POWER CONVERTER WITH DUAL MODE FEEDB ACK INPUT AND
5/24/1999	09/317348			CIRCUIT AND METHOD FOR PROTECT ING A SWITCHING POWER SUPPLY F ROM A FAULT
4/11/1979	28948	12/27/1983	4423369	INTEGRATED VOLTAGE SUPPLY METHOD FOR MAKING A
4/11/1983	484080	7/10/1984	4458408	LIGHTACTIVATED LINE-OPERABLE ZERO- CROSSING SWITCH
7/31/1981	288861	8/2/1983	4396932	METHOD FOR MAKING A LIGHT- ACTIVATED LINE-OPERABLE RO- CROSSING SWITCH INCLUDING
9/12/1979	74590	7/7/1981	4277824	START-UP CIRCUIT 5.3B VOLTAGE REGULATORS
9/12/1979	74833	11/11/1980	4233557	SWITCHING POWER SUPPLY 5.3B VOLTAGE REGULATORS
12/29/1980	220329	6/22/1982	4336586	LINEAR FULL WAVE RECTIFIER CIRCUIT 5.3E CONSUMER ENTERTAINMENT
7/14/1980	167852	2/2/1982	4314196	CURRENT LIMITING CIRCUIT 5.3B VOLTAGE AND CURRENT REGULATORS
2/4/1981	231550	11/9/1982	4358812	DRIVER CIRCUIT FOR USE WITH INDUCTIVE LOADS OR THE LIKE 5. 3F CONSUMER AUTOMOTIVE
9/12/1983	531622	2/5/1985	4498096	BUTTON RECTIFIER PACKAGE FOR NON- PLANAR DIE

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9/20/1983	534261	5/21/1985	4518982	HIGH CURRENT PACKAGE WITH MULTI-LEVEL LEADS
8/3/1994	08/285466	8/28/1995	5471167	CIRCUIT FOR USE WITH A FEEDBACK ARRANGEMENT
6/21/1999	09/337714			RAIL-TO-RAIL DRIVER FOR USE IN A REGULATOR, AND METHOD
2/5/1998	09/019292	8/31/1999	5945730	SEMICONDUCTOR POWER DEVICE
10/6/1986	915481	6/30/1987	4677368	PRECISION THERMAL CURRENT SOURCE
8/22/1989	397052	6/18/1991	5025298	SEMICONDUCTOR STRUCTURE WITH CLOSELY COUPLED SUBSTRATE TEMPERATURE SENSE
8/22/1989	396713	12/24/1991	5075259	METHOD FOR FORMING SEMICONDUCTOR CONTACTS BY ELECTROLESS PLATING
4/30/1990	516952	9/3/1991	5045964	THERMAL CLAMP FOR AN IGNITION COIL DRIVER
7/2/1999	09/346964			A LEADFRAME AND A SEMICONDUCTOR PACKAGE INCORPORATING THE LEADFRAME
1/4/1999	09/224823	1/26/1999	5973388	LEADFRAME, METHOD OF MANUFACTURING A LEADFRAME, AND METHOD OF PACKAGING AN
2/19/1999	09/255456			LEADFRAME, METHOD OF MANUFACTURING A LEADFRAME, AND METHOD OF PACKAGING AN
7/6/1999	09/347965			ELECTRONIC DEVICE PACKAGE
1/10/1994	08/179633	5/28/1996	5521488	VOLTAGE REGULATOR AND METHOD THEREFOR
4/5/1994	08/223186	7/18/1995	5434523	CIRCUIT AND METHOD FOR ADJUSTING A PULSE WIDTH OF A SIGNAL
11/27/1995	08/562865	12/22/1998	5851928	METHOD OF ETCHING A SEMICONDUCTOR SUBSTRATE
5/19/1997	08/858417			METHOD OF FORMING A CONTACT
1/8/1998	09/004656	8/31/1999	5945868	POWER SEMICONDUCTOR DEVICE AND METHOD
1/12/1999	09/229099			VARIABLE CAPACITANCE SEMICONDUCTOR DEVICE AND METHOD THEREFOR
12/21/1998	09/218250			SEMICONDUCTOR DEVICE AND METHOD OF MAKING
1/29/1981	229485	6/22/1982	4336507	CURRENT OUTPUT RELAXATION OSCILLATOR 5.3F CONSUMER -AUTOMOTIVE
3/4/1997	08/811414			ADAPTIVE EQUALIZATION CIRCUIT AND METHOD
6/30/1997	08/885500			SEMICONDUCTOR CONTACT AND METHOD THEREFOR
6/1/1998	09/087990			SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE

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5/3/1999	09/304307			CIRCUIT AND METHOD OF ACTIVATING AND DE-ACTIVATING A SWITCHING REGULATOR AT ANY
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